What is claimed is:

1. A semiconductor memory device including a plurality of memory blocks, each of the memory blocks comprising:

a memory cell array block having a plurality of word lines, a plurality of bit line pairs, and a plurality of memory cells connected between the plurality of word lines and the plurality of bit line pairs;

a write bit line pair;

a sense bit line pair;

a column selecting circuit having a plurality of first transmission transistors for transmitting data between a selected bit line pair among the plurality of the bit line pairs and the write bit line pair in response to a plurality of write control signals, and a plurality of second transmission transistors for transmitting data between the selected bit line pair and the sense bit line pair in response to a plurality of read control signals; and

a pre-charge and write control circuit for pre-charging and equalizing the sense bit line pair in response to a pre-charge enable signal during a pre-charge operation, generating the plurality of the read control signals in response to a write enable signal and a plurality of column selecting signals during a read operation, and generating the plurality of write control signals in response to a block selecting signal, the write enable signal, the pre-charge enable signal, and the plurality of the column selecting signals during a write operation.

2. The device of claim 1, wherein each of the plurality of the first transmission transistors is an NMOS transistor.

3. The device of claim 1, wherein each of the plurality of the second transmission transistors is a PMOS transistor.

4. The device of claim 1, wherein the pre-charge and write control circuit comprises:

a pre-charge and equalizing circuit for pre-charging and equalizing the sense bit line pair in response to the pre-charge enable signal;

a write signal generating circuit for generating a write signal by combining the block selecting signal, the write enable signal and the pre-charge enable signal;

a read control signal generating circuit for generating the plurality of the read control signals by combining the plurality of the column selecting signals and the write enable signal; and

a write control signal generating circuit for generating the plurality of the write control signals by combining the plurality of the column selecting signals and the write signal,

wherein all of the plurality of the first and the second transmission transistors are turned off during a pre-charge operation, and

wherein selected first transmission transistors among the plurality of the first and the second transmission transistors is turned on during a write

operation for transmitting data between the selecting bit line pair and the write bit line pair.

5. A semiconductor memory device including a plurality of memory blocks, each of the memory blocks comprising:

a memory cell array block having a plurality of word lines, a plurality of bit line pairs, and a plurality of memory cells connected between the plurality of word lines and the plurality of bit line pairs;

a write bit line pair;

a sense bit line pair;

a column selecting circuit having a plurality of first transmission transistors for transmitting data between a selected bit line pair among the plurality of bit line pairs and the write bit line pair in response to a plurality of write control signals, and a plurality of second transmission transistors for transmitting data between the selected bit line pair and the sense bit line pair in response to a plurality of read control signals; and

a pre-charge and write control circuit for equalizing the sense bit line pair in response to a pre-charge enable signal during a pre-charge operation, generating the plurality of the read control signals in response to a write enable signal, the pre-charge enable signal and a plurality of column selecting signals during a read operation, and generating the plurality of write control signals in response to a block selecting signal, the write enable signal, the pre-charge enable signal, and the plurality of the column selecting signals during a write operation.

6. The device of claim 5, wherein each of the plurality of the first transmission transistors is an NMOS transistor.

7. The device of claim 5, wherein each of the plurality of the second transmission transistors is a PMOS transistor.

8. The device of claim 5, wherein the pre-charge and write control circuit comprises:

an equalizing circuit for equalizing the sense bit line pair in response to the pre-charge enable signal;

a write signal generating circuit for generating a write signal by combining the block selecting signal, the write enable signal and the pre-charge enable signal;

a read control signal generating circuit for generating the plurality of the read control signals by combining the plurality of the column selecting signals, the write enable signal and the pre-charge enable signal; and

a write control signal generating circuit for generating the plurality of the write control signals by combining the plurality of the column selecting signals and the write signal,

wherein the plurality of the second transmission transistors are turned on during a pre-charge operation, and

wherein selected first transmission transistors among the plurality of the first and the second transmission transistors is turned on during a write operation.

9. A semiconductor memory device including a plurality of memory blocks, each of the memory blocks comprising:

a memory cell array block having a plurality of word lines, a plurality of bit line pairs, and a plurality of memory cells connected between the plurality of word lines and the plurality of bit line pairs;

a write bit line pair;

a sense bit line pair;

a column selecting circuit comprising a plurality of CMOS transmission gates, each CMOS transmission gate including an NMOS transistor connected between one of the bit lines of a bit line pair and one of the sense bit lines of the sense bit line pair, and a PMOS transistor connected between the one bit line and one of the write bit lines of the write bit line pair, the NMOS transistor and the PMOS transistor each having a control terminal; and

a pre-charge and write control circuit connected to the plurality of control terminals of the NMOS and PMOS transistors to selectively turn on and turn off the NMOS and PMOS transistors,

wherein during a write operation, the pre-charge and write control circuit turns on the NMOS transistors of a selected pair of the CMOS transmission gates, turns off the PMOS tranisistors of the selected pair of the

CMOS transmission gates, and turns off the PMOS and NMOS transistors of all of the CMOS transmission gates except the selected pair.

10. The semiconductor memory device of claim 9, wherein during a precharge operation, the pre-charge and write control circuit turns off all of the NMOS transistors and PMOS transistors of all of the CMOS transmission gates.

11. The semiconductor memory device of claim 9, wherein during a precharge operation, the pre-charge and write control circuit turns off all of the NMOS transistors and turns on all of the PMOS transistors of all of the CMOS transmission gates.